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EXAMINER	
SPITTLE, MATTHEW D	

ART UNIT	PAPER NUMBER
2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,106	JOLLY ET AL.	
	Examiner	Art Unit	
	Matthew D. Spittle	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24,26 and 27* is/are rejected.

7)☒ Claim(s) *25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 27 have been examined.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 5, 18 – 21, 26, and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Takii.

Regarding claim 1, Takii describes a circuit comprising:

A receiver (Figure 1, item 28) including an input node to receive a transfer signal (interpreted as CLOCK which comes into the input node of item 28 in Figure 1), and an output node to pass only the transfer signal from the input node to the output node (where the output node is interpreted as the output of Figure 1, item 28);

A signal detector connected to the receiver (Figure 1, item 44) to generate an internal signal (Figure 1, item MISSING CLOCK DETECT) based on the transfer signal, wherein the signal detector is configured to hold the internal signal at a first signal level when the transfer signal repeatedly switches between the first signal level and a second signal level, and wherein the signal detector is configured to hold the internal signal at a second signal level when the transfer signal stops switching (Figure 2, items A, E).

Regarding claim 2, Takii describes wherein signal detector includes a detect circuit to detect for changes in voltage levels represented by the transfer signal (Examiner interprets the timer (Figure 1, item 44) as containing a detect circuit since it is responsive to changes in voltages as shown in Figure 2).

Regarding claim 3, Takii describes wherein signal detector further includes a switching circuit to switch the internal signal between the first and second signal levels (Examiner interprets the timer (Figure 1, item 44) as containing a switching circuit since it switches the signal levels as shown in Figure 2 (item MISSING CLOCK DETECT)).

Regarding claim 4, Takii describes wherein signal detector further includes a holding circuit to hold the internal signal at one of the first and second signals (Examiner interprets the timer (Figure 1, item 44) as containing a holding circuit since it is capable of holding the signal at a high level as shown in Figure 2 (item MISSING CLOCK DETECT)).

Regarding claim 5, Takii describes an integrated circuit comprising:

A plurality of terminals (Examiner notes that electronic devices such as logical gates, flip-flops, timers, etc inherently have I/O terminals to permit connection to other devices. Therefore, the output of AND gate (Figure 1, item 24) could have a terminal, as well as the input to flip flop (Figure 1, item 36).

A number of transmitters connected to a first group of terminals of the plurality of terminals to transmit signals to the first group of terminals (Examiner notes that since AND gate (Figure 1, item 24) transmits a signal from its output, it could be interpreted as a transmitter. Similarly, NOT gate (Figure 1, item 28) could also be considered a transmitter since it also transmits a signal from its output).

A number of receivers (Figure 1, items 18, 14, 44) connected to a second group of terminals (Examiner interprets TIMERs (Figure 1, items 44, 14) as containing input terminals since they are electronic devices.) of the plurality of terminals to receive signals from the second group of terminals;

A signal detector (Figure 1, item 44) connected to at least one of the receivers to control an internal signal (Figure 1, item MISSING CLOCK DETECT) based on a transfer signal (interpreted as CLOCK which comes into and out of item 28 in Figure 1) received from a selected terminal of the second group of terminals (the CLOCK signal is received at the input terminal of item 44) by one of the receivers (Figure 1, item 44), wherein the signal detector is configured to switch the internal signal from a first signal level to a second signal level when the transfer signal repeatedly switches between the first and second signal levels, and wherein the signal detector is configured to switch the internal signal from the second signal level back to the first signal level when the transfer signal stops switching (Figure 2, items A, E).

Regarding claim 18, Takii describes a method comprising:

Receiving a transfer signal (interpreted as CLOCK which comes into the input node of item 28 in Figure 1) at an input node of a receiver and passing only the transfer signal from the input node to an output node of the receiver (where the output node is interpreted as the output of Figure 1, item 28);

Monitoring the transfer signal (Examiner interprets monitoring to mean "detecting and responding to changes," since TIMER (44) responds to changes in the transfer signal, Examiner finds it to meet this limitation.)

Holding an internal signal at a first signal level when the transfer signal stays at one of the first signal level and a second signal level;

Holding the internal signal at a second signal level when the transfer signal repeatedly switches between the first and second signal levels;

Switching the internal signal from the second signal level to the first signal level when the transfer signal stops switching (Figure 2, items A, E).

Regarding claim 19, Takii describes holding the internal signal at the first signal level after the transfer signal stops switching (Figure 2, items A, E).

Regarding claim 20, Takii describes wherein monitoring includes detecting for changes in signal levels of the transfer signal (Examiner interprets TIMER (44) to meet this limitation since it clearly is responsive to changes in signal levels as shown in Figure 2, items A, E).

Regarding claim 21, Takii implicitly describes wherein one of the first signal level and the second signal level represents one of a voltage level and ground (Examiner notes that since Takii describes his system as one relating to the digital arts (column 1, lines 22 – 26), it refers to digital signals which are well known to consist of logical 1's and 0's, or, electrically speaking, a voltage level and ground).

Regarding claim 26, Takii describes wherein holding the internal signal at the first signal level occurs when the transfer signal stays at one of the first and second signal levels for a time interval equal to at least one cycle of the transfer signal (Figure 2, items A, E).

Regarding claim 27, Takii describes wherein holding the internal signal at the second signal level occurs when the transfer signal repeatedly switches between the first and second signal levels such that the transfer signal has at least two consecutive cycles (Figure 2, items A, E).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 6 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takii in view of Janus et al.

With regard to claim 6, Takii fails to teach the transmitters and receivers configured to transfer data via the terminals according to peripheral component interconnect (PCI) express standard.

Janus et al. teach using the peripheral component interconnect express standard (paragraph 19).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the PCI express standard as taught by Janus et al. into the invention of Takii for the purpose of transmitting and receiving data on a bus. This would have been obvious since Janus et al. teach that the PCI express architecture has the advantages of low pin count, and high speed, serial device-to-device interconnect.

With regard to claim 7, Takii fails to teach the transmitters and receivers configured to transfer data via the terminals according to serial digital video output (SVDO) standard.

Janus et al. teach using the serial digital video output standard (paragraph 20).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the SVDO standard as taught by Janus et al. into the invention of Takii for the purpose of connecting a display device. This would have been obvious since Janus et al. teach that SVDO devices can generate digital display signals to drive a display monitor (paragraph 23).

With regard to claim 8, Takii fails to teach the transmitters and the receivers configured to transfer data via the terminals according both a peripheral component interconnect (PCI) express standard and a serial digital video output (SDVO) standard.

Janus et al. teach using both a PCI express standard and SDVO standard (paragraphs 19, 20).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate both the PCI express and SDVO standards for the purposes as described above. Additionally, this would have been obvious since Janus et al. teach that SDVO and PCI express signals are physically and electrically compatible (paragraph 28).

* * *

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takii in view of Oh.

Regarding claim 9, Takii fails to teach a transmitting circuit including:

An input node to receive a send signal having the first and second signal levels;

An output node to transfer the transfer signal to the selected terminal of the second group of terminals, wherein the transmitting circuit is configured to hold the transfer signal at one of the first and second signal levels when the send signal has the first signal level, and wherein the transmitting circuit repeatedly switches the transfer signal between the first and second signal levels when the send signal has the second signal level.

Oh teaches a transmitting circuit including:

An input node (Figure 3, item 22) to receive a send signal (Figure 3, item STP_HCLK) having the first and second signal levels (Figure 4, item STP_HCLK);

An output node (interpreted as the output of Figure 3, item 22) to transfer the transfer signal (Figure 3, item Host Bus Clock) to the selected terminal of the second group of terminals, wherein the transmitting circuit (Figure 3, item 220) is configured to hold the transfer signal at one of the first and second signal levels when the send signal has the first signal level, and wherein the transmitting circuit repeatedly switches the transfer signal between the first and second signal levels when the send signal (Figure 4, item STP_HCLK) has the second signal level (Figure 4, item Host Bus Clock).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to combine the clock detecting means of Takii with the bus system of Oh for the purpose of allowing both clock and data to share the same signal line in the system of Oh. This would make it possible to reduce the size of, and consequently the cost, of the system of Oh.

* * *

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takii in view of Schoenborn.

Regarding claim 10, Takii teaches a system comprising:

A plurality of connectors, each of the connectors including a number of pins (Examiner notes that electronic devices such as logical gates, flip-flops, timers, etc inherently have connectors with pins to permit connection to other devices. Therefore, the AND gate (Figure 1, item 24) could have a connector with pins, as well as the flip flop (Figure 1, item 36);

A chipset including a chipset interface connected to at least one of the connectors, the chipset interface including:

A plurality of terminals connected to at least one of the connectors ((Examiner notes that electronic devices such as logical gates, flip-flops, timers, etc inherently have I/O terminals to permit connection to other devices. Therefore, the output of AND gate

(Figure 1, item 24) could have a terminal, as well as the input to flip flop (Figure 1, item 36).

A plurality of transmitters connected to the terminals (Examiner notes that since AND gate (Figure 1, item 24) transmits a signal from its output, it could be interpreted as a transmitter. Similarly, NOT gate (Figure 1, item 28) could also be considered a transmitter since it also transmits a signal from its output).

A plurality of receivers connected to the terminals (Examiner interprets TIMERs (Figure 1, items 44, 14) as containing input terminals since they are electronic devices.)

A signal detector (Figure 1, item 44) connected to at least one of the receivers to hold an internal signal (Figure 1, item MISSING CLOCK DETECT) at a first signal level based on a presence of a repeated switching of a transfer signal (interpreted as CLOCK which comes into and out of item 28 in Figure 1) among the input signals, and to hold the internal signal at a second signal level based on an absence of the repeated of switching of the transfer signal (Figure 2, items A, E).

Takii fails to teach using differential signals in the transmitters and receivers.

Schoenborn teach using differential signals on a bus for the purpose of reducing clock skew, reducing electromagnetic interference, ensuring signal integrity, and lower power consumption (column 6, lines 23 – 42).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate differential signals as taught by Schoenborn in the system of Takii for the purpose of reducing clock skew, reducing electromagnetic

interference, ensuring signal integrity, and lower power consumption. This would have been obvious in order to make the system more reliable and reduce its operating costs.

* * *

Claims 11 – 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takii in view of Janus et al.

With regard to claim 11, Takii fails to teach the transmitters and receivers configured to transfer data via the terminals according to peripheral component interconnect (PCI) express standard.

Janus et al. teach using the peripheral component interconnect express standard (paragraph 19).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the PCI express standard as taught by Janus et al. into the invention of Takii for the purpose of transmitting and receiving data on a bus. This would have been obvious since Janus et al. teach that the PCI express architecture has the advantages of low pin count, and high speed, serial device-to-device interconnect.

With regard to claim 12, Takii fails to teach the transmitters and receivers configured to transfer data via the terminals according to serial digital video output (SVDO) standard.

Janus et al. teach using the serial digital video output standard (paragraph 20).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the SVDO standard as taught by Janus et al. into the invention of Takii for the purpose of connecting a display device. This would have been obvious since Janus et al. teach that SVDO devices can generate digital display signals to drive a display monitor (paragraph 23).

With regard to claim 13, Takii fails to teach wherein the interface of the chipset is configured to drive a digital display monitor.

Examiner takes official notice that it would be obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate a digital display monitor in the system of Takii for the purpose of displaying relevant status information, debugging information, etc. This is evidenced by Naoe (column 5, line 61 – column 6, line 10).

With regard to claim 14, Takii fails to teach a card having a number of pins connected to one of the connectors.

Examiner takes official notice that it would be obvious to one of ordinary skill in this art at the time of invention by applicant to implement part or all of the circuit of Takii on a card, also known as a printed circuit board, printed wire board, or other electrical equivalent that would resemble a card-like shape for the purpose of providing a means of mounting individual electrical components and a means of transferring signals between them.

* * *

Claims 15 – 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takii in view of Oh.

Regarding claim 15, Takii fails to teach a transmitting circuit including:

An input node to receive a send signal having the first and second signal levels;

An output node to transfer the transfer signal to the selected terminal of the second group of terminals, wherein the transmitting circuit is configured to hold the transfer signal at one of the first and second signal levels when the send signal has the first signal level, and wherein the transmitting circuit repeatedly switches the transfer signal between the first and second signal levels when the send signal has the second signal level.

Oh teaches a transmitting circuit including:

An input node (Figure 3, item 22) to receive a send signal (Figure 3, item STP_HCLK) having the first and second signal levels (Figure 4, item STP_HCLK);

An output node (interpreted as the output of Figure 3, item 22) to transfer the transfer signal (Figure 3, item Host Bus Clock) to the selected terminal of the second group of terminals, wherein the transmitting circuit (Figure 3, item 220) is configured to hold the transfer signal at one of the first and second signal levels when the send signal has the first signal level, and wherein the transmitting circuit repeatedly switches the

transfer signal between the first and second signal levels when the send signal (Figure 4, item STP_HCLK) has the second signal level (Figure 4, item Host Bus Clock).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to combine the clock detecting means of Takii with the bus system of Oh for the purpose of allowing both clock and data to share the same signal line in the system of Oh. This would make it possible to reduce the size of, and consequently the cost, of the system of Oh.

With regard to claim 16, Takii fails to teach a motherboard in which the connectors and the chipset are located.

Examiner takes official notice that it would be obvious to one of ordinary skill in this art at the time of invention by applicant to implement the circuit as taught by Takii on a motherboard for the purpose of providing a means of mounting individual electrical components and a means of transferring signals between them.

Regarding claim 17, Takii teaches the additional limitation of a processor connected to one of the connectors (Figure 1, item 44; Examiner interprets TIMER (44) as a processor, since it receives an input and provides a processed output (MISSING CLOCK DETECT).

* * *

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takii in view of Oh.

Regarding claim 22, Takii fails to teach wherein the transfer signal is generated based on a send signal, wherein each of send signal and the internal signal has a frequency lower than the frequency of the transfer signal.

Oh teaches wherein the transfer signal (Figure 3, item Host Bus Clock) is generated based on a send signal (Figure 3, item STP_HCLK), wherein each of send signal and the internal signal has a frequency lower than the frequency of the transfer signal (Examiner notes that as shown in Figure 4, the send signal (STP_HCLK) clearly has a frequency lower than the frequency of the transfer signal (Host Bus Clock). Furthermore, Examiner notes that in Figure 2 of Takii, the internal signal (E) clearly has a frequency lower than the frequency of the transfer signal (A)).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to combine the clock detecting means of Takii with the bus system of Oh for the purpose of allowing both clock and data to share the same signal line in the system of Oh. This would make it possible to reduce the size of, and consequently the cost, of the system of Oh.

* * *

Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takii in view of Oh.

Regarding claim 23, Takii teaches a method comprising:

Monitoring the transfer signal (Examiner interprets monitoring to mean "detecting and responding to changes," since TIMER (44) responds to changes in the transfer signal, Examiner finds it to meet this limitation.)

Holding an internal signal at a first signal level when the transfer signal stays at one of the first signal level and a second signal level;

Holding the internal signal at a second signal level when the transfer signal repeatedly switches between the first and second signal levels;

Switching the internal signal from the second signal level to the first signal level when the transfer signal stops switching (Figure 2, items A, E).

Takii fails to teach wherein the transfer signal is generated based on a send signal, wherein each of send signal and the internal signal has a frequency lower than the frequency of the transfer signal, and wherein the transfer signal repeatedly switches between the first and second signal levels when the send signal has the first signal level.

Oh teaches wherein the transfer signal (Figure 3, item Host Bus Clock) isbased on a send signal (Figure 3, item STP_HCLK), wherein each of send signal and the internal signal has a frequency lower than the frequency of the transfer signal (Examiner notes that as shown in Figure 4, the send signal (STP_HCLK) clearly has a frequency lower than the frequency of the transfer signal (Host Bus Clock). Furthermore,

Examiner notes that in Figure 2 of Takii, the internal signal (E) clearly has a frequency lower than the frequency of the transfer signal (A)), and wherein the transfer signal repeatedly switches between the first and second signal levels when the send signal has the first signal level (Figure 4, item Host Bus Clock).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to combine the clock detecting means of Takii with the bus system of Oh for the purpose of allowing both clock and data to share the same signal line in the system of Oh. This would make it possible to reduce the size of, and consequently the cost, of the system of Oh.

Regarding claim 24, Oh teaches the additional limitation wherein the transfer signal stops switching when the send signal level has the second signal level (Figure 4, item Host Bus Clock).

Allowable Subject Matter

Claim 25 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record neither teaches nor suggests all of the claimed subject matter of claim 25 including "wherein send signal and the internal signal have the same frequency."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MDS

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